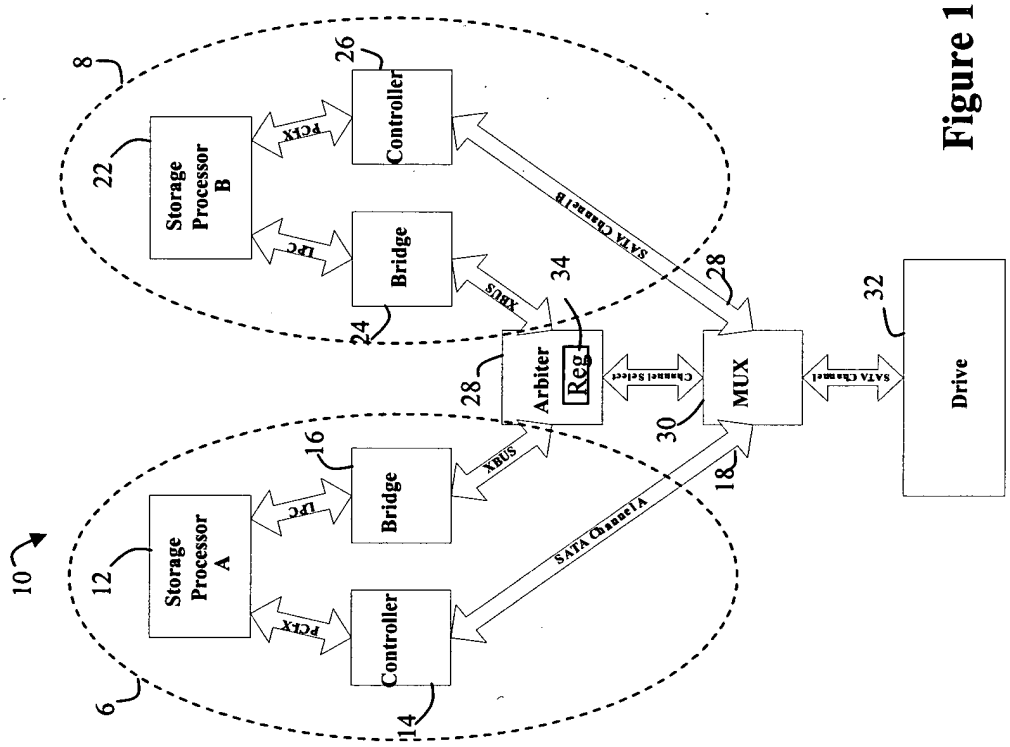
8
26
Controller
PCIX
22
Storage Processor B
LPC
Bridge
24
SATA Channel B
XBUS
34
28
32
28
Arbiter
Reg
Channel Select
MUX
SATA Channel
Drive
30
18
16
XBUS
LPC
Bridge
SATA Channel A
10
12
Storage Processor A
PCIX
Controller
6
14

Figure 1

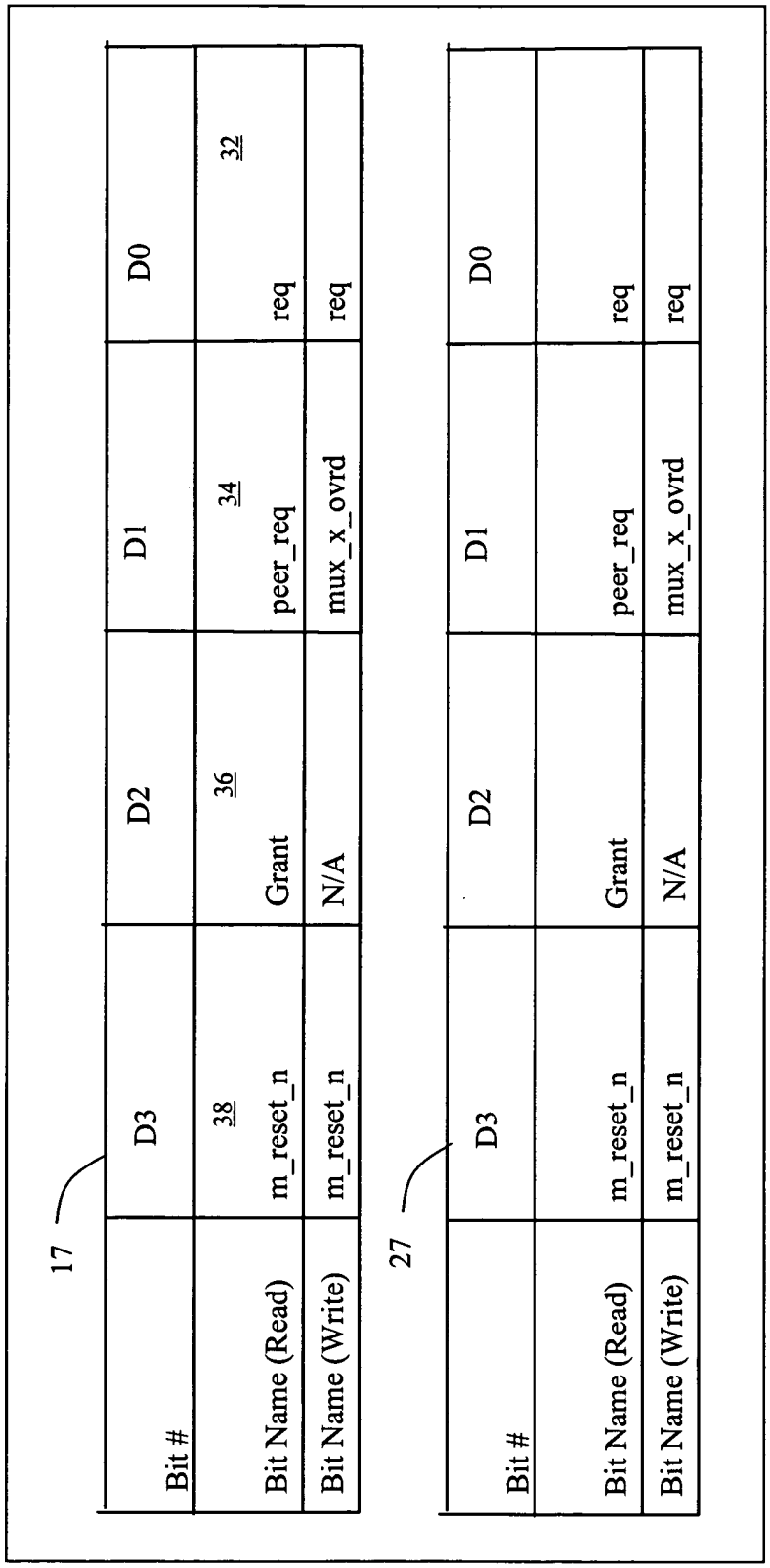
34 Mux Control Registers
17
27
Bit #
D3
D2
D1
D0
Bit Name (Read)
38
m_reset_n
36
Grant
34
peer_req
32
req
Bit Name (Write)
m_reset_n
N/A
mux_x_ovrd
req

Figure 2

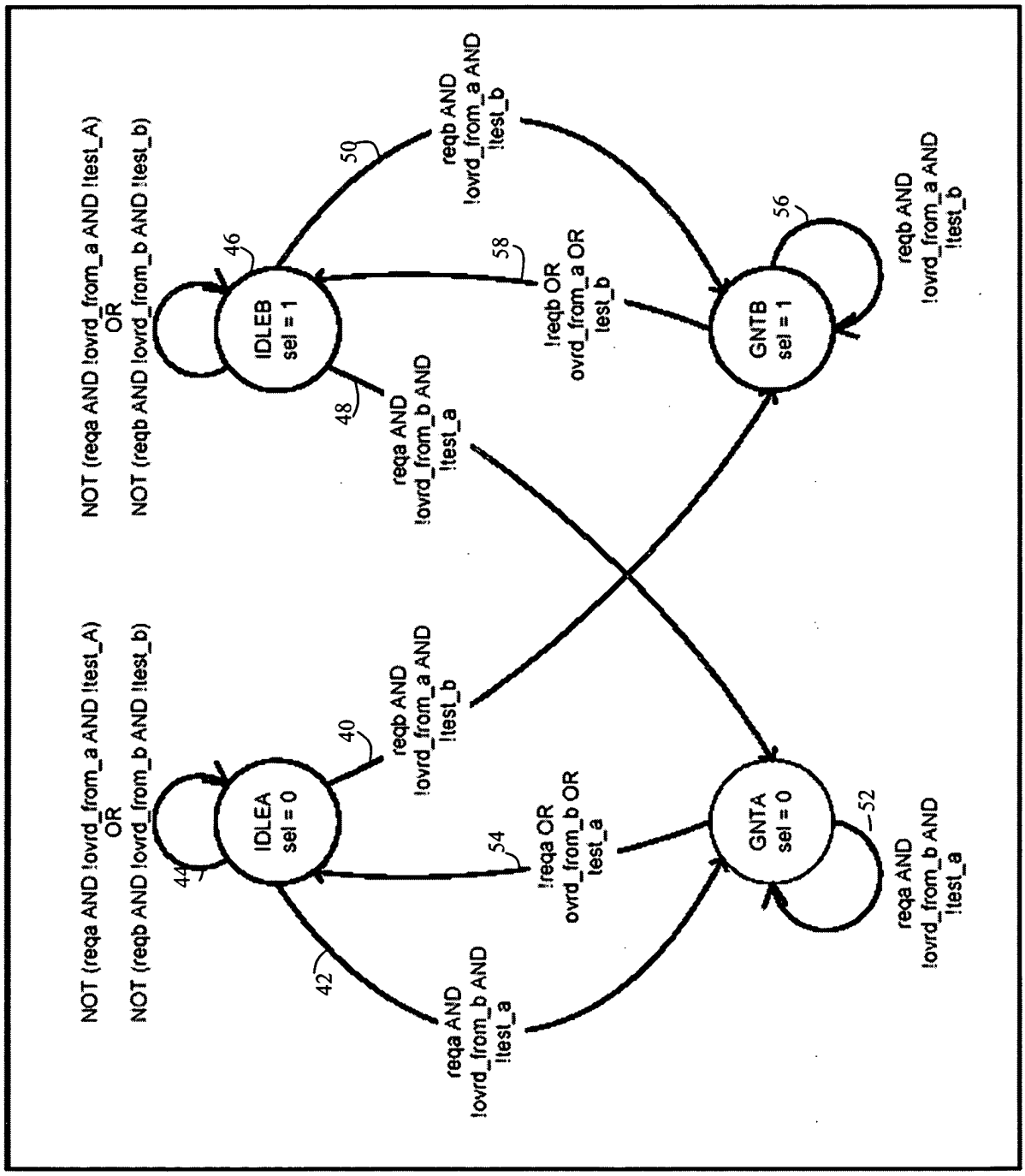
IDLEA
sel = 0
IDLEB
sel = 1
GNTA
sel = 0
GNTB
sel = 1
40
42
44
46
48
50
52
54
56
58
NOT (reqa AND !ovrd_from_a AND !test_A) OR NOT (reqb AND !ovrd_from_b AND !test_b)
reqb AND !ovrd_from_a AND !test_b
reqa AND !ovrd_from_b AND !test_a
!reqa OR ovrd_from_b OR test_a
!reqb OR ovrd_from_a OR test_b

Figure 3